

CURRENTLY AVAILABLE PROCESSORS

Manufacturer	Family	Chip, Core, or Both	Arithmetic	Data Width (bits)	Instruction Width (bits)	Maximum Instruction Clock Speed [1]	Relative DSP Speed BDTImark2000™ [2,5]	Total External Addressable Memory Space [3]	Core Voltage(s) [5]	Unit Price [4,5] (Qty. 10,000)	Notes
3DSP	SP-5	Core	Fixed-point	32	32	150 MHz	n/a	4G	2.5	CV	Dual-issue superscalar DSP
Analog Devices	ADSP-21xx	Chip	Fixed-point	16	24	75 MHz	230	16K - 32K	2.5, 3.3, 5.0	\$5 - 68	Many family members w/ assorted peripherals
	ADSP-219x	Chip	Fixed-point	16	24	160 MHz	n/a	16M	2.5	\$45	Enhanced version of the ADSP-21xx
	ADSP-2106x	Chip	Floating-pt.	32	48	66 MHz	250	64M - 4G	3.3, 5.0	\$20 - 445	Strong support for multiprocessor designs
	ADSP-2116x	Chip	Floating-pt.	32	48	80 MHz	410	4G	2.5	\$99	SIMD-enhanced ADSP-2106x
DSP Group	OakDSPCore	Core	Fixed-point	16	16	80 MHz	n/a	128K	CV	CV	Successor to DSP Group's Pine; widely licensed
	TeakLiteDSPCore	Core	Fixed-point	16	16	225 MHz	n/a	128K	CV	CV	Faster Oak
	TeakDSPCore	Core	Fixed-point	16	16	210 MHz	n/a	4M	CV	CV	Dual MAC units, synthesizable core
	PalmDSPCore	Core	Fixed-point	16/20/24	16/32	210 MHz	n/a	16M	CV	CV	Selectable data width, dual MAC, synthesizable
Hitachi	SH2-DSP	Chip	Fixed-point	16	16/32	100 MHz	280	16M - 64M	3.3	CV	Hybrid DSP/microcontroller based on SH-2
	SH3-DSP	Chip	Fixed-point	16	16/32	187 MHz	460	384M	3.3	CV	Hybrid DSP/microcontroller based on SH-3
Infineon	TriCore	Both	Fixed-point	32	16/32	80 MHz	n/a	4G	2.5	CV	Dual-issue hybrid DSP/microcontroller core
	Carmel	Core	Fixed-point	16	24/48	250 MHz	1850	8M	2.5	CV	6-way VLIW, customizable instructions
LSI Logic	LSI40xZ (ZSP core)	Both	Fixed-point	16	16	200 MHz	n/a	1M	2.5	CV	4-way superscalar architecture
	LX5280	Core	Fixed-point	32	16/32	185 MHz	790	8G	1.8	CV	MIPS-compatible core with DSP extensions
Lucent Technologies	DSP16xxx	Chip	Fixed-point	16	16/32	170 MHz	810	64K	1.8, 2.5, 3.3	\$40 - 90	Dual-MAC architecture
	StarPro2000	Chip	Fixed-point	16	16	300 MHz	n/a	512M	1.5	CV	Chip based on three StarCore SC140 cores
Motorola	DSP563xx	Chip	Fixed-point	24	24	150 MHz	450	16M	1.8, 2.5, 3.3	\$8 - 52	PCI bus, DMA, can run '560xx code unmodified
	DSP568xx	Chip	Fixed-point	16	16	40 MHz	110	0 - 64K	3.0 - 3.6	\$6 - 16	Contains many microcontroller-like features
	MSC8101	Chip	Fixed-point	16	16	300 MHz	3430	4G	1.5	\$96	Chip based on a single StarCore SC140 core
Texas Instruments	TMS320C2xxx	Chip	Fixed-point	16	16	40 MHz	n/a	192K	3.3, 5.0	\$3 - 15	Low-cost cross between 'C2x and 'C5x
	TMS320C3x	Chip	Floating-pt.	32	32	75 MHz	n/a	16M	1.8	\$10 - 178	Cost-competitive with fixed-pt DSPs
	TMS320C54xx	Chip	Fixed-point	16	16	160 MHz	500	0 - 8M	1.2, 1.5, 1.8, 2.5, 3.3, 5.0	\$5 - 84	Many specialized instructions
	TMS320C55xx	Chip	Fixed-point	16	8 - 48	160 MHz	n/a	16M	1.6	\$29	2-way VLIW based on 'C54xx architecture
	TMS320C62xx	Chip	Fixed-point	16	32	300 MHz	1920	8M	1.5, 1.8	\$29 - 201	8-way VLIW
	TMS320C67xx	Chip	Floating-pt.	32	32	167 MHz	820	8M	1.8, 1.9	\$17 - 139	Floating-point version of 'C62xx

FORTHCOMING PROCESSORS [6]

Analog Devices	TigerSHARC	Chip	Fixed/Float	8/16/32/40	32	120 MHz	n/a	4G	1.8	\$150	4-way VLIW with SIMD capabilities
Motorola	DSP5685x	Chip	Fixed-point	16	16	120 MHz	n/a	16M	1.8	\$3.75 - 4.50	Enhanced version of the '568xx
Texas Instruments	TMS320C28xx	Core	Fixed-point	32	16	400 MHz	n/a	8G	1.8	CV	Hybrid microcontroller/DSP
	TMS320C64xx	Chip	Fixed-point	8/16	32	600 MHz	n/a	1.5G	1.2	CV	Next generation of 'C6xxx architecture

Notes [1] Instruction clock speed for fastest member of family. Most processors issue one instruction per clock cycle; VLIW and superscalar processors may issue multiple instructions. [2] The BDTImark2000 is a summary measure of DSP speed; higher is faster. BDTImark2000 scores are not comparable to earlier BDTImark scores published by BDTI. See www.BDTI.com for additional BDTImark2000 scores. [3] Chips: off-chip addressable memory space; Core/Both: core addressable memory space. (In native words.) [4] Unit prices quoted by manufacturers as of June, 2000. [5] CV = Contact vendor; n/a = information not available [6] Data is projected; processor has not yet been fabricated or is not yet available at speed shown.

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